

# Solutions - Midterm Exam

(February 19<sup>th</sup> @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (15 PTS)

a) Complete the following table. The decimal numbers are unsigned: (6 pts.)

Decimal	BCD	Binary	Reflective Gray Code
89	10001001	1011001	1110101
119	000100011001	1110111	1001100
76	01110110	1001100	1101010
135	000100110101	10000111	11000100

b) Complete the following table. Use the fewest number of bits in each case: (7 pts.)

REPRESENTATION			
Decimal	Sign-and-magnitude	1's complement	2's complement
-89	11011001	10100110	10100111
52	0110100	0110100	0110100
-51	1110011	1001100	1001101
-20	110100	101011	101100
-64	11000000	10111111	1000000

c) Convert the following decimal numbers to their 2's complement representations. (2 pts)

✓ -16.1875

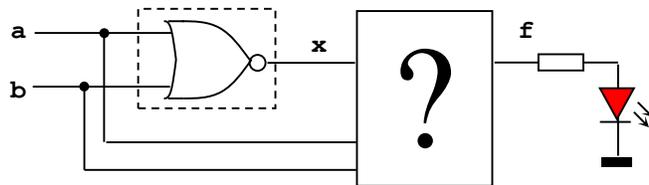
+16.1875 = 010000.0011  
⇒ 101111.1101

✓ 37.3125

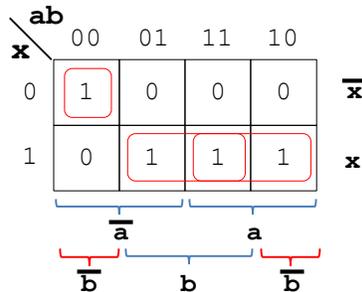
+37.3125 = 0100101.0101

## PROBLEM 2 (20 PTS)

a) Using only 2-to-1 MUXs, design a circuit that verifies the logical operation of a NOR gate.  $f = '1'$  (LED ON) if the NOR gate does NOT work properly.  
Assumption: when the NOR gate is not working, it generates 1's instead of 0's and vice versa.  
Tip: Minimize your function first. (15 pts)



a	b	x	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

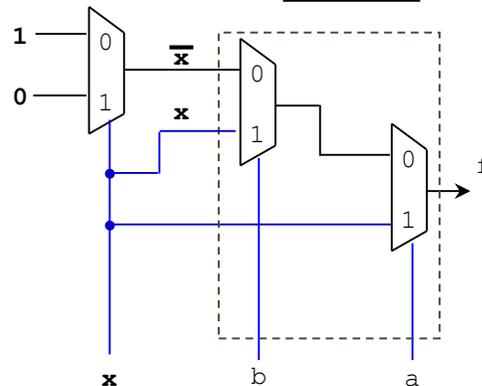


$$f = \bar{a}\bar{b}\bar{x} + bx + ax$$

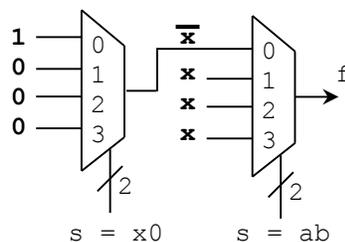
$$f(a,b,x) = \bar{a}f(0,b,x) + af(1,b,x) = \bar{a}(\bar{b}\bar{x} + bx) + a(bx + x) = \bar{a}(\bar{b}\bar{x} + bx) + a(x) = \bar{a}g(b,x) + ax$$

$$g(b,x) = \bar{b}g(0,x) + bg(1,x) = \bar{b}(\bar{x}) + b(x)$$

$$\text{Also: } \bar{x} = \bar{x}(1) + x(0)$$



b) Implement the previous function  $f$  using only 4-to-1 MUXs. You might need to implement a NOT gate using a 4-to-1 MUX.



### PROBLEM 3 (10 PTS)

- The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte.  $1\text{KB} = 2^{10}$  bytes,  $1\text{MB} = 2^{20}$  bytes,  $1\text{GB} = 2^{30}$  bytes
  - What is the size of the memory space? What is the address bus size of the microprocessor?

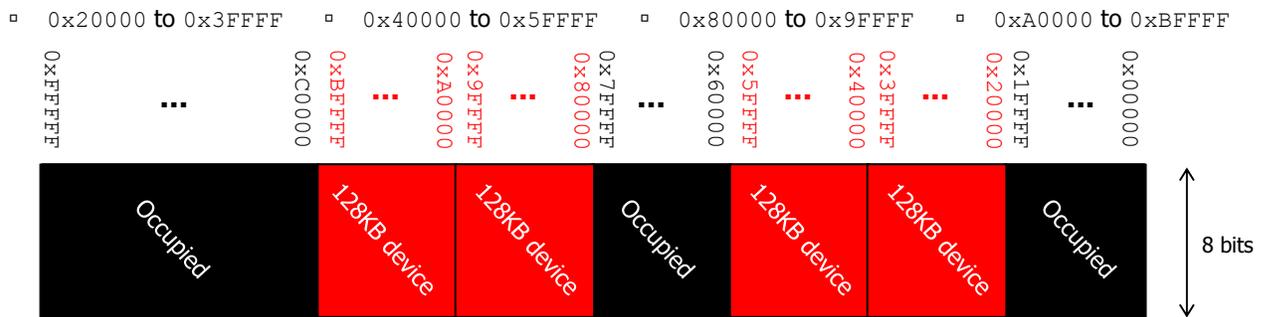
Address space:  $0x00000$  to  $0xFFFFF$ . To represent all these addresses, we require 20 bits. So, the address bus size of the microprocessor is 20 bits. The size of the memory space is then  $2^{20} = 1\text{MB}$ .

- If we have a memory chip of 128KB, how many bits do we require to address those 128KB of memory?

128 KB memory device:  $128\text{KB} = 2^{17}$  bytes. Thus, we require 17 bits to address the memory device.

- We want to connect the 128KB memory chip to the microprocessor. The figure shows all the occupied portions of the memory space. Provide a list of all the possible ranges that the 128 KB memory chip can occupy.

128KB of memory require 17 bits. The 17-bit address range would be from  $0x00000$  to  $0x1FFFF$ . Within the entire 20-bit memory space, there are four options to place those 128KB in the figure:



### PROBLEM 4 (20 PTS)

- a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits  $n$  to represent both operators. Indicate every carry (or borrow) from  $c_0$  to  $c_n$  (or  $b_0$  to  $b_n$ ). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (8 pts)

✓  $51 + 15$

$$\begin{array}{r}
 \overset{c_6}{1} \overset{c_5}{1} \overset{c_4}{1} \overset{c_3}{1} \overset{c_2}{1} \overset{c_1}{1} \overset{c_0}{0} \\
 51 = 0x33 = 1\ 1\ 0\ 0\ 1\ 1\ + \\
 15 = 0x0F = 0\ 0\ 1\ 1\ 1\ 1 \\
 \hline
 \text{Overflow!} \rightarrow 1\ 0\ 0\ 0\ 0\ 1\ 0
 \end{array}$$

✓  $25 - 35$

$$\begin{array}{r}
 \text{Borrow out!} \rightarrow \overset{b_6}{1} \overset{b_5}{0} \overset{b_4}{0} \overset{b_3}{0} \overset{b_2}{1} \overset{b_1}{0} \overset{b_0}{1} \\
 25 = 0x19 = 0\ 1\ 1\ 0\ 0\ 1\ - \\
 35 = 0x23 = 1\ 0\ 0\ 0\ 1\ 1 \\
 \hline
 0x36 = 1\ 1\ 0\ 1\ 1\ 0
 \end{array}$$

- b) Perform the following operations, where numbers are represented in 2's complement. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)

✓  $-89 + 128$

$n = 9$  bits

$$\begin{array}{r}
 \overset{c_8}{1} \overset{c_7}{1} \overset{c_6}{0} \overset{c_5}{0} \overset{c_4}{0} \overset{c_3}{0} \overset{c_2}{0} \overset{c_1}{0} \overset{c_0}{0} \\
 -89 = 1\ 1\ 0\ 1\ 0\ 0\ 1\ 1\ 1\ + \\
 128 = 0\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0 \\
 \hline
 39 = 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 1 \\
 -89 + 128 = 39 \in [-2^8, 2^8-1] \rightarrow \text{no overflow}
 \end{array}$$

$c_9 \oplus c_8 = 0$   
No Overflow

✓  $-61 - 13$

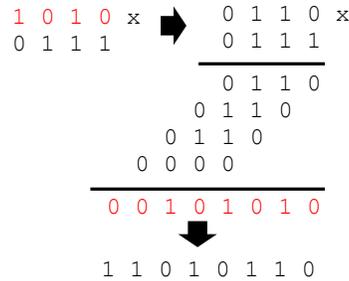
$n = 7$  bits

$$\begin{array}{r}
 \overset{b_6}{1} \overset{b_5}{0} \overset{b_4}{0} \overset{b_3}{0} \overset{b_2}{0} \overset{b_1}{1} \overset{b_0}{1} \\
 -61 = 1\ 0\ 0\ 0\ 0\ 1\ 1\ + \\
 -13 = 1\ 1\ 1\ 0\ 0\ 1\ 1 \\
 \hline
 0\ 1\ 1\ 0\ 1\ 1\ 0 \\
 -61 - 13 = -74 \notin [-2^6, 2^6-1] \rightarrow \text{overflow!}
 \end{array}$$

To avoid overflow:  $n = 8$  bits (sign-extension)

$$\begin{array}{r}
 \overset{c_7}{1} \overset{c_6}{1} \overset{c_5}{0} \overset{c_4}{0} \overset{c_3}{0} \overset{c_2}{0} \overset{c_1}{1} \overset{c_0}{1} \\
 -61 = 1\ 1\ 0\ 0\ 0\ 0\ 1\ 1\ + \\
 -13 = 1\ 1\ 1\ 1\ 0\ 0\ 1\ 1 \\
 \hline
 -74 = 1\ 0\ 1\ 1\ 0\ 1\ 1\ 0 \\
 -61 - 13 = -74 \in [-2^7, 2^7-1] \rightarrow \text{no overflow}
 \end{array}$$

- c) Get the multiplication result of the following numbers that are represented in 2's complement arithmetic with 4 bits. (4 pts)  
 $\checkmark 7 \times -6.$

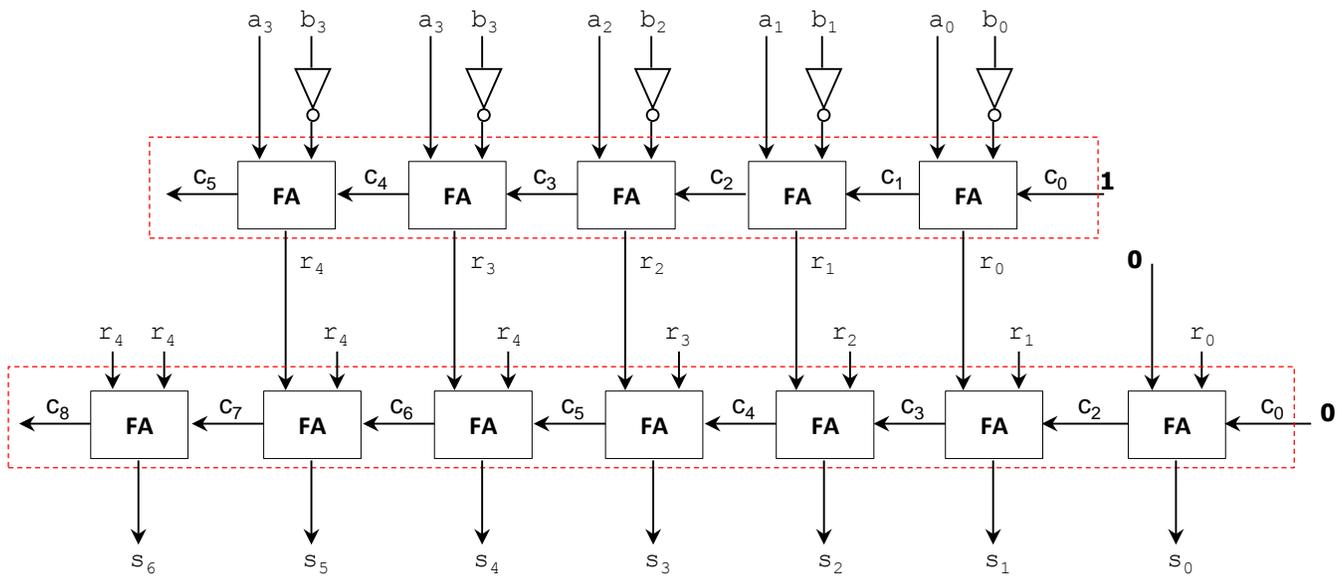


**PROBLEM 5 (10 PTS)**

- Given two 4-bit signed (2's complement) numbers A, B, sketch the circuit that computes  $(A - B) \times 3$ . You can use full adders and logic gates. Make sure your circuit avoids overflow.
- BONUS POINTS (+2 PTS): Use the fewest amount of hardware resources.

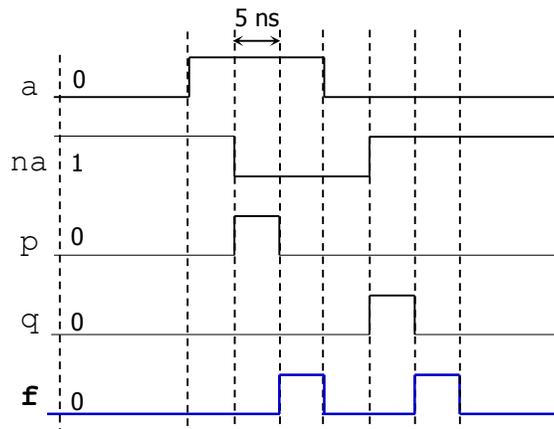
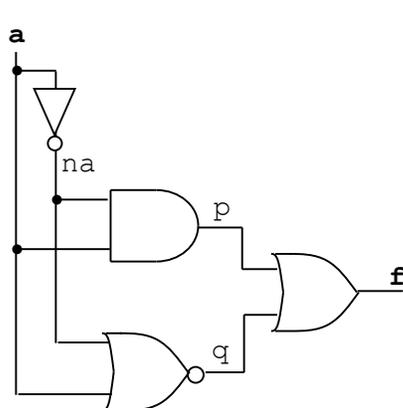
$$(A - B) \times 3 = (A - B) \times 2 + (A - B)$$

Worst case:  $15 \times 3 = 45$ . 45 requires 7 bits, therefore, we need to sign extend  $(A - B) \times 2$  on the last addition.



**PROBLEM 6 (10 PTS)**

- Complete the timing diagram of the digital circuit shown below. You must consider the propagation delays. Assume the propagation delay of every gate is 5 ns. The initial values of all signals are plotted in the figure.



PROBLEM 7 (15 PTS)

- Complete the timing diagram of the circuit shown below:

